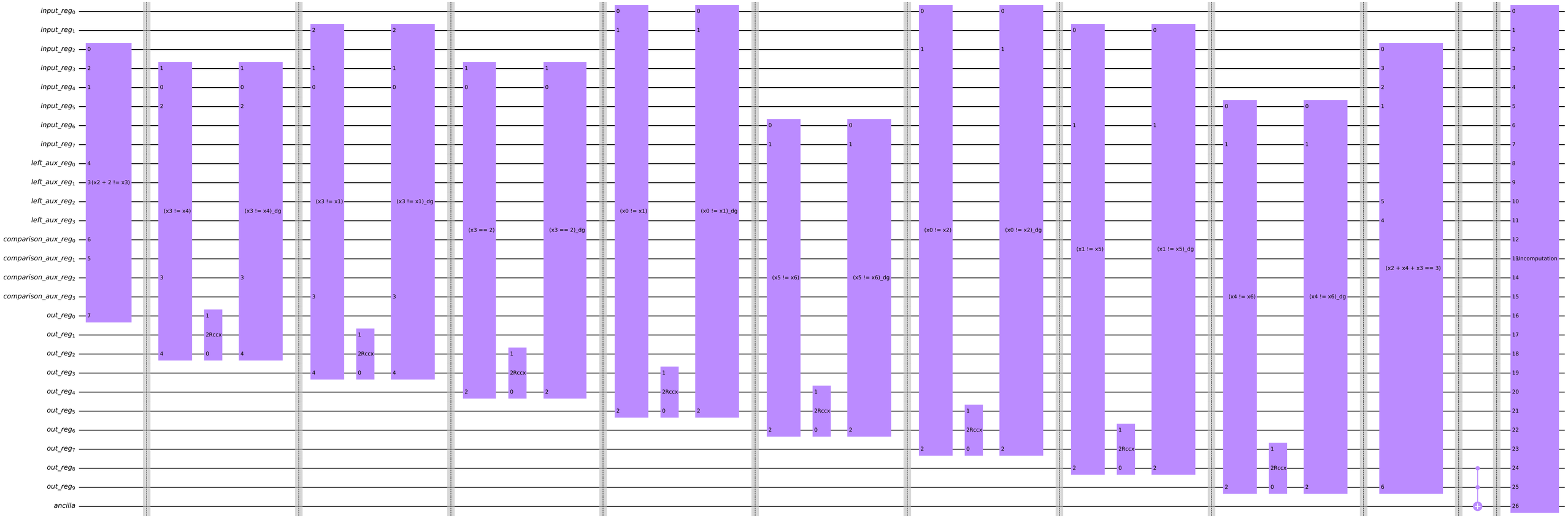
input_reg0
input_reg1
input_reg2
input_reg3
input_reg4
input_reg5
input_reg6
input_reg7
left_aux_reg0
left_aux_reg1
left_aux_reg2
left_aux_reg3
comparison_aux_reg0
comparison_aux_reg1
comparison_aux_reg2
comparison_aux_reg3
out_reg0
out_reg1
out_reg2
out_reg3
out_reg4
out_reg5
out_reg6
out_reg7
out_reg8
out_reg9
ancilla
(x2 + 2 != x3)
(x3 != x4)
2Rccx
(x3 != x4)_dg
(x3 != x1)
2Rccx
(x3 != x1)_dg
(x3 == 2)
2Rccx
(x3 == 2)_dg
(x0 != x1)
2Rccx
(x0 != x1)_dg
(x5 != x6)
2Rccx
(x5 != x6)_dg
(x0 != x2)
2Rccx
(x0 != x2)_dg
(x1 != x5)
2Rccx
(x1 != x5)_dg
(x4 != x6)
2Rccx
(x4 != x6)_dg
(x2 + x4 + x3 == 3)
Incomputation